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Design and Simulation of Logic Circuits at Nano Scale Beyond 32 Nano Meters (FinFet)

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ABSTRACT- With advancement in electronic circuitry, efforts are made to minimize chip size and to attain the desired performance so on changing one parameter the other parameters are effected like variables of field effect transistor like length and width are key variables available to the circuit designer to optimize circuit performance .When in FET's like CMOS (complementary metal oxide semiconductor) the dimensions are decreased, the short channel effect arises and creates a problem of concern. With this effect an exponential increase in the leakage current happens. In order to reduce the SCE and hence leakage current, a new technology came into being in recent years in which a 3D multiple gate CMOS like FinFet (Fin Field Effect Transistor) has been developed which possess advantages over conventional FET's and has attracted many engineers and designers to make it more sophisticated. This technology works in the nano meter range to minimize short channel effects. Many companies like Intel, advanced micro device, global foundries have started using FinFet technology. I have carried out my work on the basis of current researches on FinFet technology and how FinFet technology can be used in future to design new logic and memory devices like Inverter, MUX etc. Various parameters of FinFet like reduced short channel effects, less leakage current, low power consumption, less propagation delay and less time delay are discussed. Various mathematical models and software were used to simulate power, delay, power delay product, average power dissipation and energy delay products, this technology was designed to eliminate the problem of SCE by permitting transistors to be scaled down into sub 20nm range. Use of PMT model to design different logic devices at 16nm technology and analyzed output of each circuit. Parameters like Power dissipation, time delay and PDP were compared between MOSFET (CMOS) technology and FinFet technology for each circuit.

KEYWORDS- CMOS, Logic Circuits, FinFet, Short Channel Effect, VLSI

I. INTRODUCTION

With the passage of time chip density and operating frequency got increased, as nanometer process technologies have advanced, making power utilization in battery operated and devices a major issue (because of the need of increased packaging and cooling cost). So, for the designers of VLSI[12] (Very Large Scale Integration) the main goal is to fulfill performance requirements within a power requirement. Hence there is an increased importance of power efficiency. In FinFet technology, which is an emerging technology, offering interesting power delay trade-offs, is likely to augment CMOS (Complementary metal Oxide semiconductor) [17], when scaled down to 32nm and beyond.

In design metrics, we have performance, area, cost and time to open-air market. Since the beginning of the Integrated Circuit industry, the desire to optimize this design metrics has not changed. Moore's law, in fact is all about optimizing these parameters. However, as scaling continued, and the manufacturing nodes progressed towards 20nm, some parameters especially the power supply voltage, which is the main factor in determining the dynamic power could not be scaled any further. One more issue was, optimizing in one variable demands in big compromises in other variables, for example, performance optimization caused degradation in power factor. Hence the design window was shrinking for optimizing among the design variables aforementioned. But FinFet broadens the design window once again[1]. Dynamic and static power was saved significantly as operating voltage continues scaling down. Short cannel effects are reduced significantly. Hence continuing to improve performance compared to planar device at an identical node. Performance advantages of the FinFet [9][6][5] widens compared to its planar equivalent, because of superior gate control of the channel in FinFet.As compared to its planar counterpart, one major design optimization benefits of FinFets the fact that it gives much higher performance at the very same power budget, or at a much minimum power budget it provides equal performance. Hence giving the designers and engineers the potential to extract the higher performance for the minimum power, which is a much-needed requirement for devices which operate on batteries. In VLSI, thousands of circuits based on transistors which are connected and combined to create integrated circuits (IC's). Examples of VLSI device are microprocessor, microcontroller. In present era, VLSI architectures are used in the manufacturing of almost each and every chip today[2]. To meet these demands size, efficiency and power consumption must be reduced. For the design of both analog and dialog circuits, power dissipation is the most important objective to be optimized. By using the

FinFet technology as compared to the circuits implemented in CMOS, the average leakage power, the clock power, and the total active mode power consumption are reduced up to 53%, 29%, and 55% respectively for the combinational circuits, while maintaining similar data stability and speed.

II. MATERIALS AND METHODS

To increase the speed and performance of integrated circuits many ways have been tried by the researchers. Due to which the number of transistors per integrated circuit or chip get increased by two times every year following the well-known Moore's law. This rise in the of transistors count has been achieved either by increasing the chip's size or by minimizing the transistor size. However, minimizing the transistor size is the main reason to increased chip density. We have seen that as device size is scaled down to 28nm, researchers face lot of barriers related to the its fabrication and characteristics. At that small dimension transistor performance is affected by short channel effects. The Short channel effect causes an exponential increase in the leakage current between the source and drain terminal even when the device is off, causing the gate to lose control over channel to such an extent that it cannot turn off the channel completely. This and other technical challenges drove researchers to go for alternative transistor designs .Thus, FinFet technology was designed to eliminate the problem of SCE by permitting transistors to be scaled down into sub 20nm range.

As the dimensions of MOSFET[19] (Metal Oxide Semiconductor Field Effect Transistor) decreases, the short channel effect(SCE) becomes a dominating concern and leads to increase in leakage current and thus power dissipation increases. In order to reduce leakage current, hence power dissipation a new technology, known as FinFet technology has been proposed to design logical devices. Different devices like Inverter, Adder and MUX etc[4]. have been designed using both CMOS and FinFet technology to compare various parameters like power dissipation, delay and power delay product. Here in this research we have tried to design these circuits at channel length of 16nm using spice software. So, this paper compares FinFet technology with CMOS technology

III. DESIGN OF LOGIC AND MEMORY CIRCUITS

First, we designed all the circuits using CMOS[22] technology at 16nm channel length and the values of different parameters have been calculated as mentioned in table 1. Also, we used PTM model in design and simulation of all the circuits Again, using FinFet technology all the above circuits at 16nm channel length have been designed. After designing, the Voltage transient characteristics have been obtained for each circuit using Spice Simulator tool. And different parameters like power dissipation and time delay have been calculated as shown in table 1,2 respectively. The output waveforms of all the above designed gates and circuits are shown in figures[19][6]. All of the figures show the input and output waveforms generated from the HSPICE simulation. The output of all the devices produced are as expected in the truth table as tabulated in Table1.

IV. DESIGN OF INVERTER

This is the most basic gate, with one input and one output. It produces a '1' output if the input is '0' and vice-versa. That is, it produces an inverted version of the input at its output. That is why it is also known as Inverter. The symbol of NOT gate is given in figure 1.

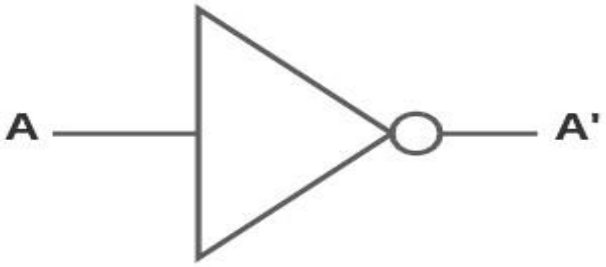


Figure. 1: NOT gate

The Boolean expression for NOT (inverter) gate is A = A' When A=1, we get 0 as output and when A=0, we get 1 as output i.e., we get opposite of input as output in inverter or NOT gate. The truth table for inverter in shown in table 1.

Table 1: Truth table of NOT gate

A	A'
0	1
1	0

The design of CMOS inverter is shown in figure 2 and the design of FinFet inverter in figure 3

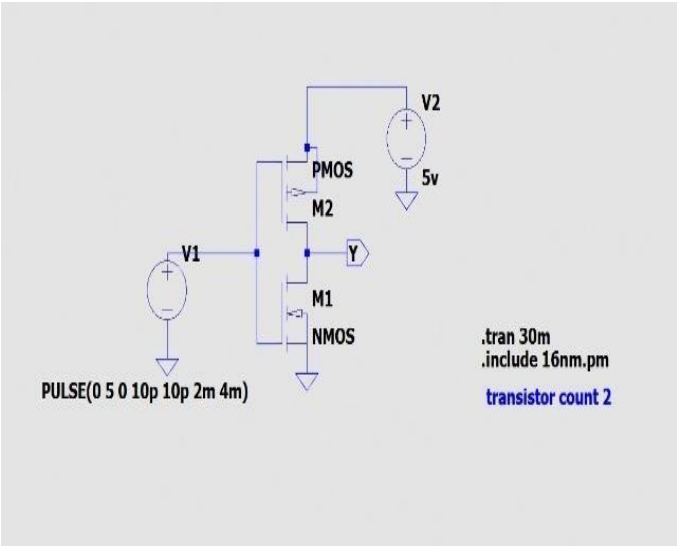


Figure 2: Inverter using CMOS logic

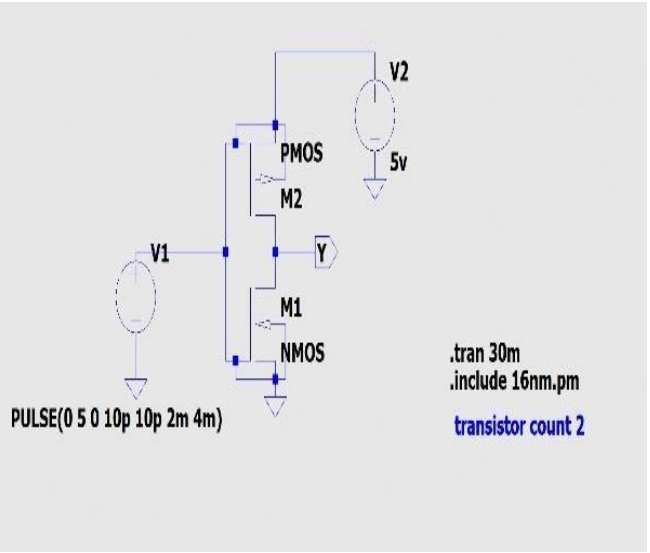


Figure 3: Output waveform of Inverter

We used HSPICE software, for design of inverter of 16nm channel length and then simulated the circuit using PTM model[7][8].

Output waveform of Inverter in figure 4.

Figure 4: Output waveform of Inverter

V. DESIGN OF HALF ADDER

It is a combinational circuit and performs addition of two binary numbers and gives Sum & Carry as output. Its Truth Table and gate level representation is given below in table 2 and figure 5 respectively.

The value of Sum ranges from 0 to 2 in decimal for addition of two bits. So, we need two bits for representing it in binary system. [5]

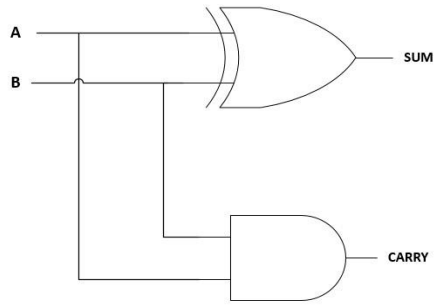


Figure 5: Half Adder using Logic gates

The Boolean expression for Half adder

$S = A \cdot B + A \cdot B$

$C = A \cdot B$

Table 2: Truth table of Half adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The Half Adder using CMOS logic is represented in figure 6 and Half Adder using FinFet technology is in figure 7[13].The wave form of Half Adder is represented in figure 8.

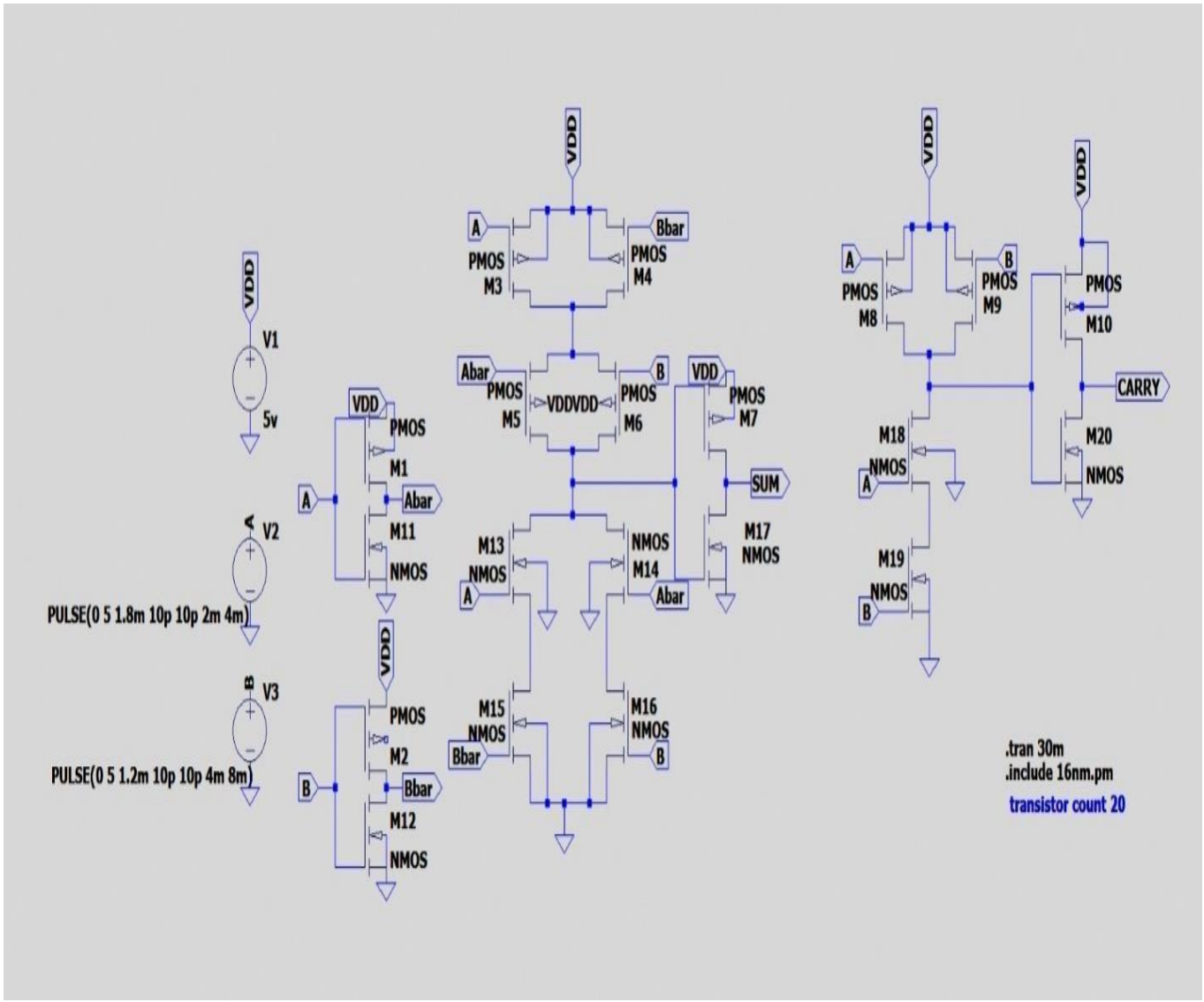


Figure 6: Half Adder using CMOS logic

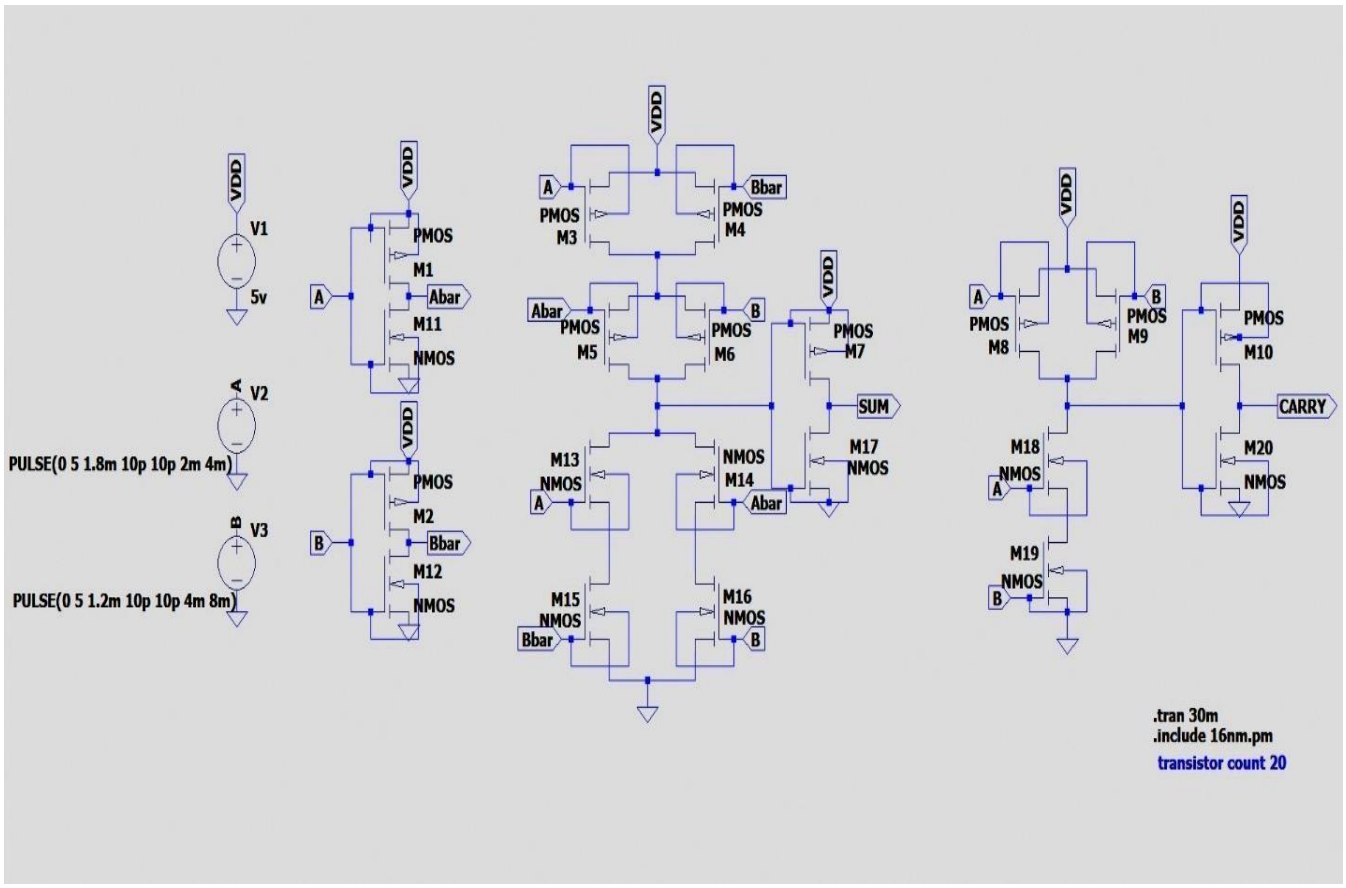


Figure 7: Half Adder using FinFet technology

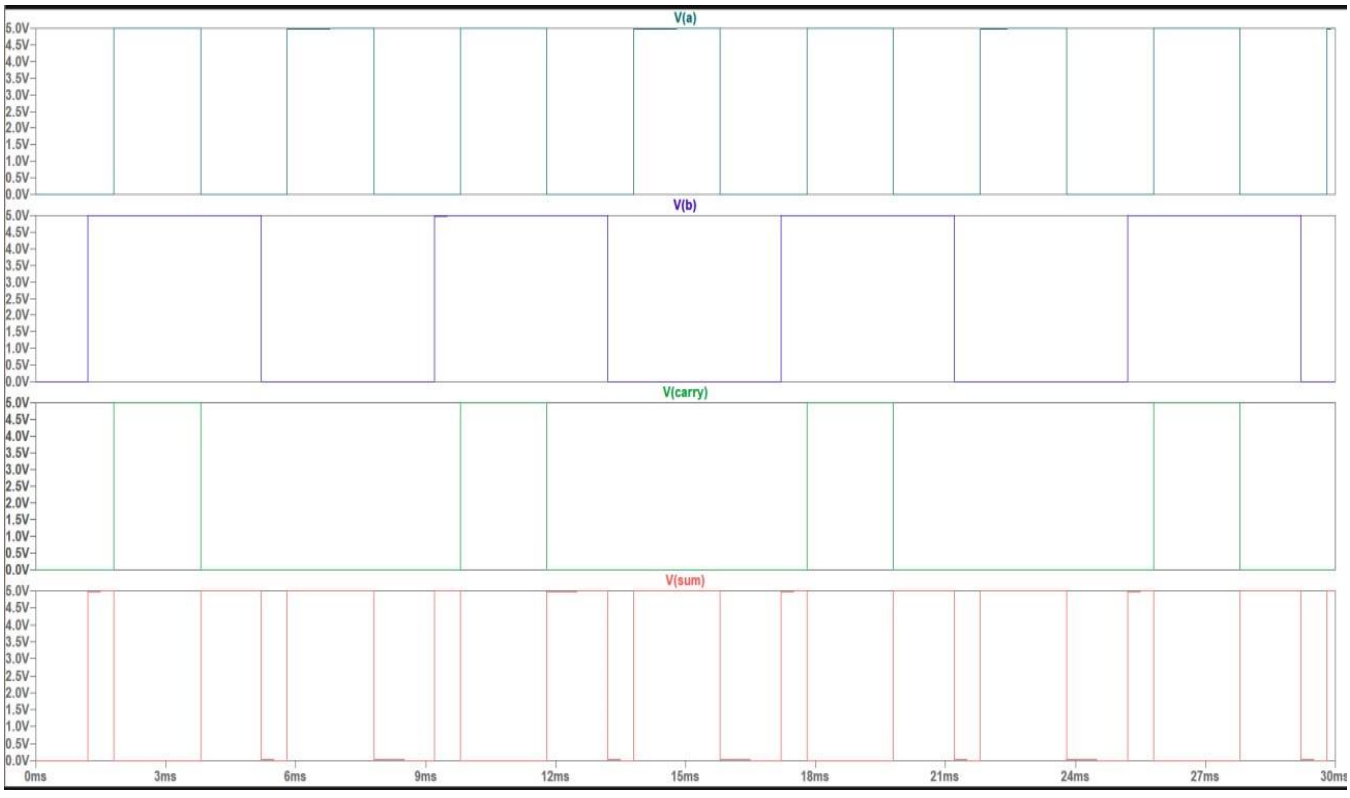


Figure 8: Waveform of Half Adder

VI. DESIGN OF 2:1 MUX

Multiplexer, also known as data selector is a device that selects between several analog or digital signals and forwards the selected input to a single output line(Fig 9). The selection is directed by a separate set of digital inputs known as select lines, say S1 and S2. A multiplexer of 2n inputs has n select lines, which are used to select which input line to send to the output. Multiplexer can be of different types depending on number of inputs like 2:1 MUX ,4:1 MUX. Etc. but, in our research, we have worked upon 2:1 MUX. The block diagram of 2:1 MUX is shown in figure. I0 and I1 are the two inputs and S0 is the select line which selects among I0 and I1 and send to the output 'f'. The design of 2:1 MUX using logic gates is shown in figure 10.

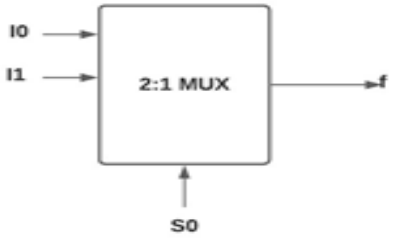


Figure 9: Block diagram of 2:1 MUX

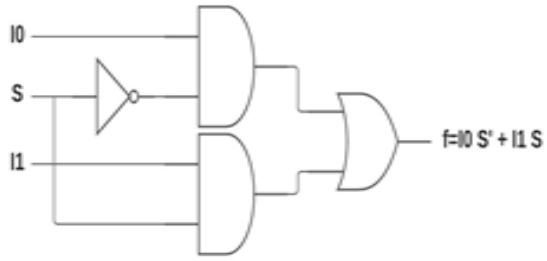


Figure 10: 2:1 MUX using logic gates

The design of 2:1 MUX is shown in figure 11 using CMOS and the design of 2:1 MUX is shown in figure 12 using FinFet technology and figure 13 represents waveform of 2:1 MUX.

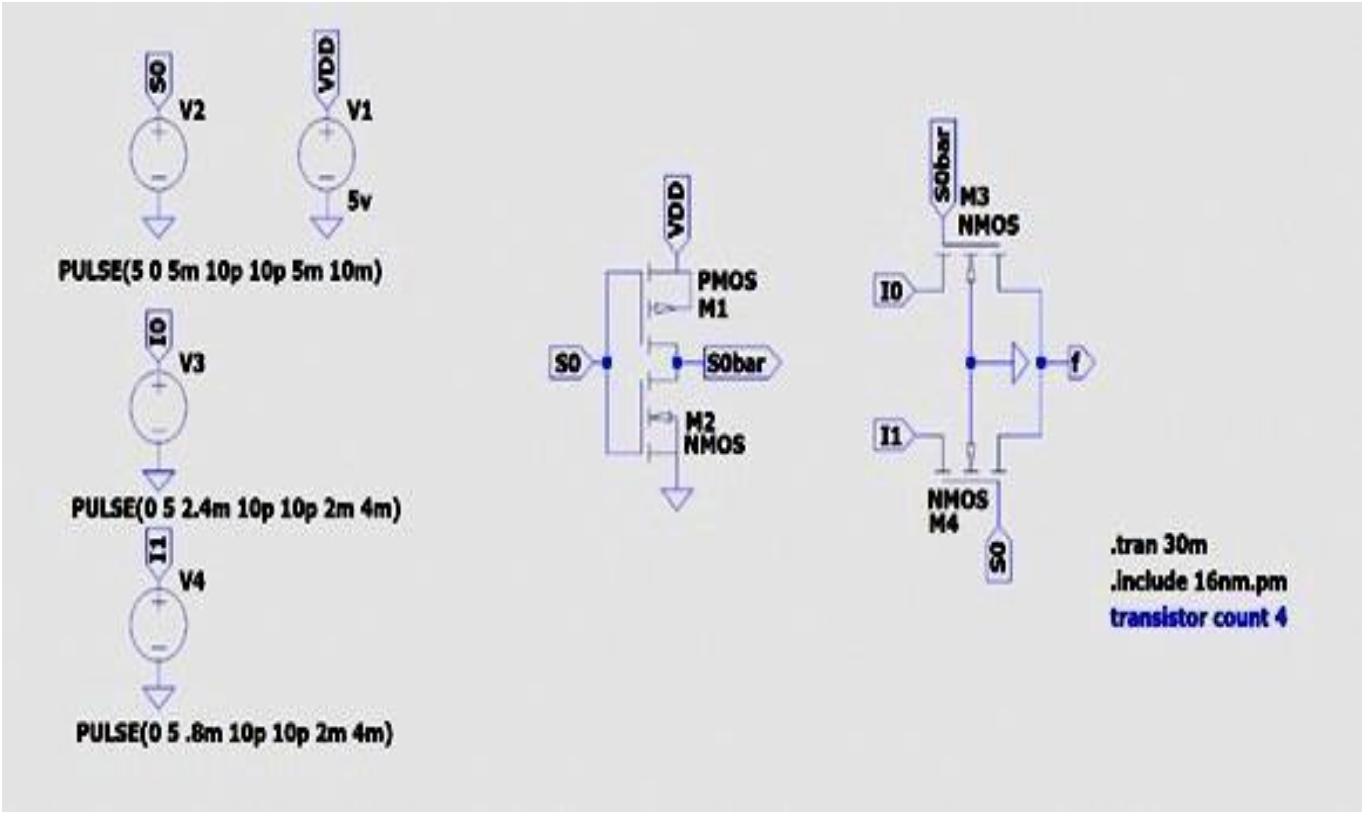


Figure 11: 2:1 MUX using CMOS logic

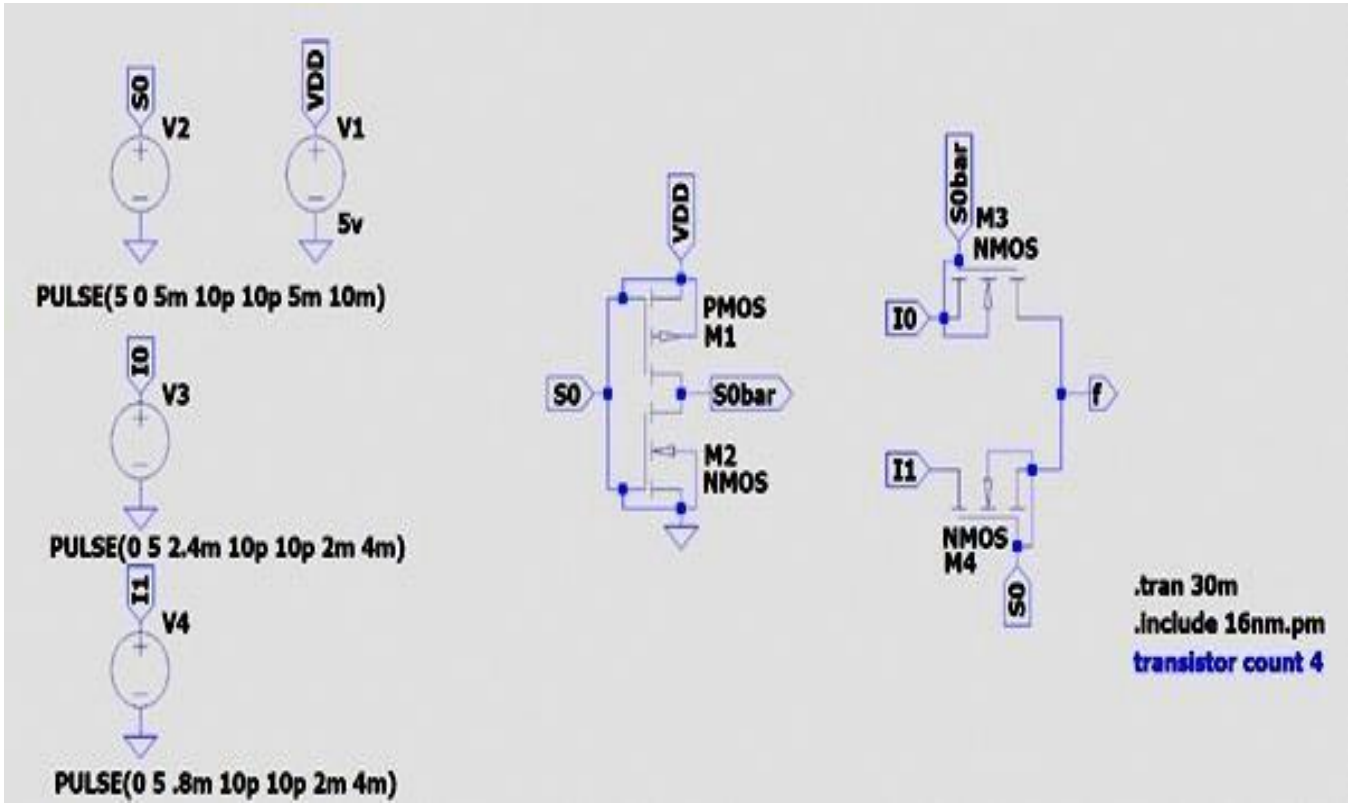


Figure 12: 2:1 MUX using FinFet technology

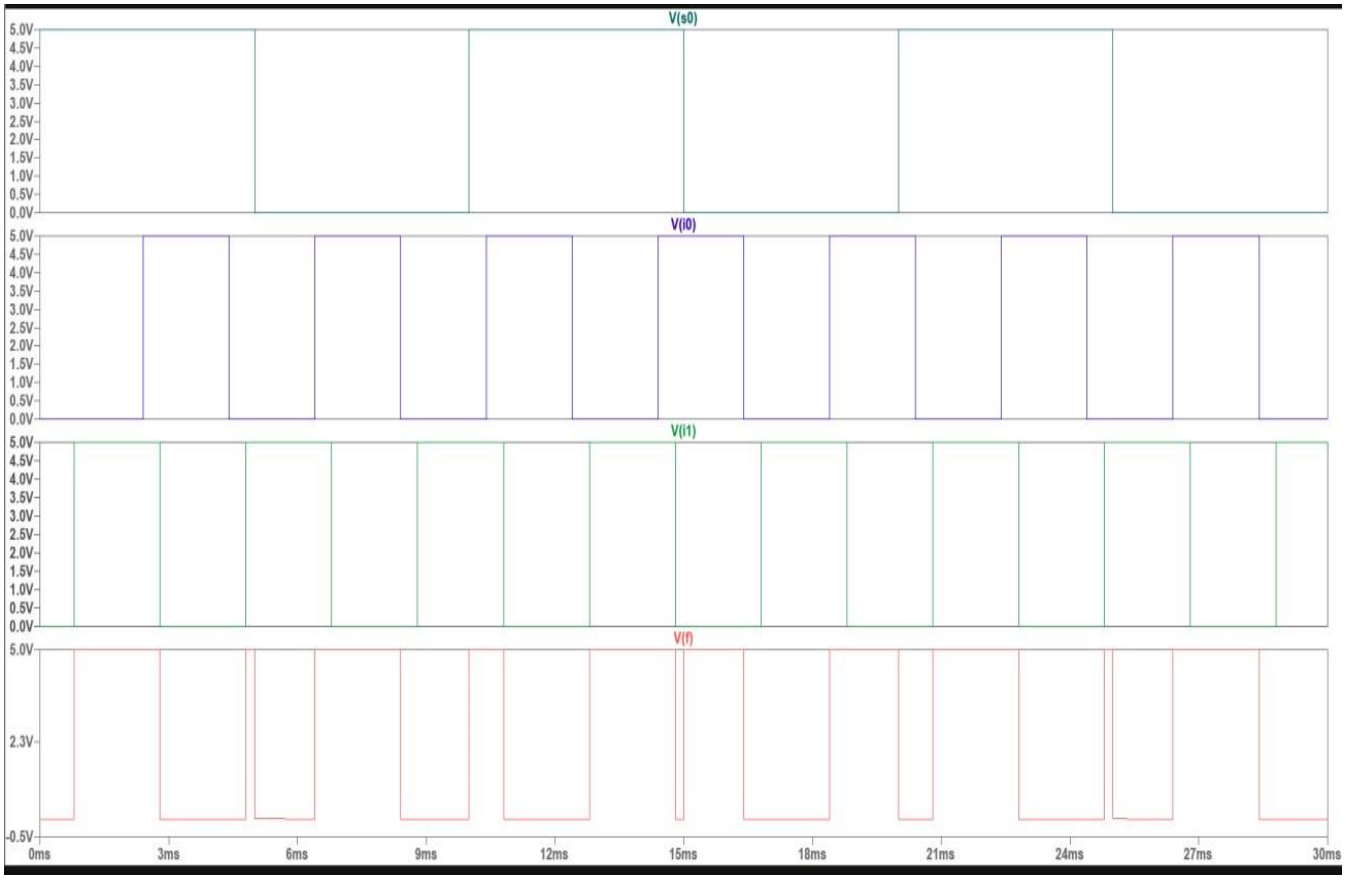


Figure 13: Waveform of 2:1 MUX

VII. RESULTS

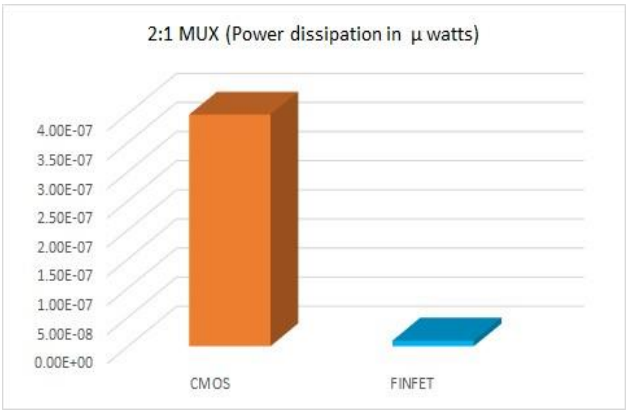
Table 3: Power Dissipation comparison between CMOS and FinFet.

DEVICE	MOSFET TECHNOLOGY	FinFet Technology
INVERTER	402.123n	497.736f
Half Adder	0.5233µ	119.5p
2:1 MUX	397.87n	9.8n

The figures a,b,c, depicts the variation of output voltage with respect to time which help us to find out average power dissipation and time delay at 16nm channel length, maintaining the same power supply as mentioned in table 1 & 2.

Following graphs gives clear view of the power dissipation and time delay comparison between MOSFET and FinFet based circuits[14]. Here we can clearly relate the power dissipation and time delay in each circuit based on both CMOS [11]and FinFet technology. Power dissipation is more in COMOS based circuits than FinFet based circuits so CMOS based circuits consume more power as compared to FinFet circuits. Also time delay calculated in micro seconds is more in CMOS circuits than FinFet circuits. First six figures depict relation of power dissipation in each circuit designed using both CMOS[21] and FinFet technology [16]and the last six figures shows time delay of each circuit designed using both the technologies[19].

(a)



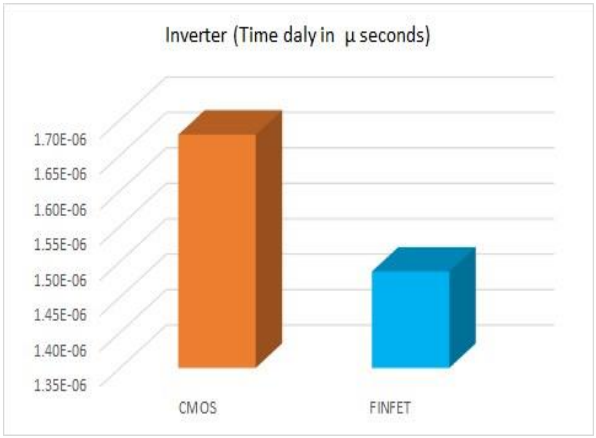
(b)

Figure. 14: Power Dissipation of (a) Inverter (b) Half Adder, (c) 2:1 MUX.

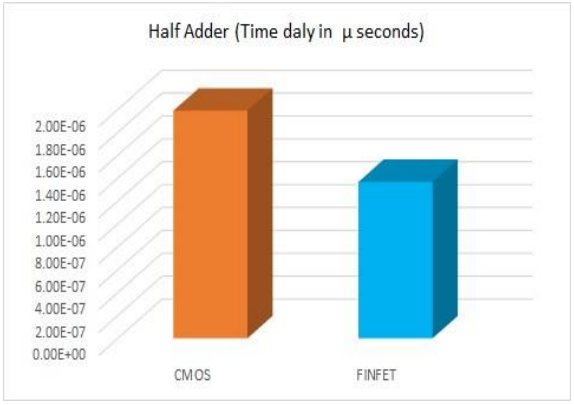
Figure 14 is showing the output variations in inverter (a)half Adder (b) and mux.

Table 4: Time Delay comparison between CMOS and FinFet

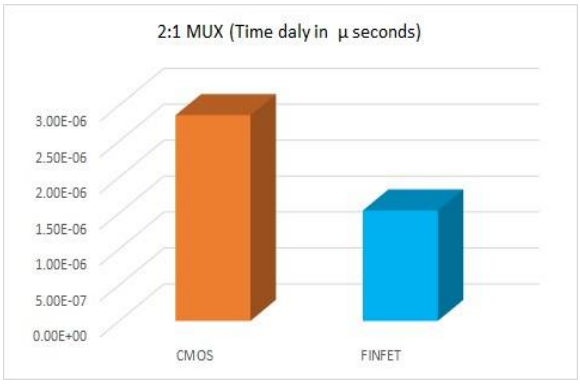
DEVICE	MOSFET	FINFET
INVERTER	1.679µ	1.486µ
Half Adder	1.989µ	1.367µ
2:1 MUX	2.861µ	1.536µ



(a)



(b)



(c)

Figure 15: shows Time Delay of (a) Inverter, (b) Half Adder, (c) 2:1 MUX.

VIII. CONCLUSION AND FUTURE WORK

As we have seen in this thesis work, FinFets offer far superior results as compared to the conventional MOSFETs[12]. The power dissipation and time delays occurring due to the circuits based on FinFets has been drastically lowered. Power consumption and time delays are among the most important parameters in checking the performance of a digital circuit, especially in those devices which are portable and require batteries to operate. As per the designs space offered by the FinFet devices, it is very much possible that FinFet devices will replace the conventional transistors under the technology node of 16nm and beyond.

Due to their ease of fabrication process, and much better performance, FinFet is emerging as a very good option in replacing the conventional transistors. As compared to the conventional transistors, the fabrication process of FinFets is almost similar.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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