International Journal of Innovative Research in Engineering & Management (IJIREM)
ISSN: 2350-0557, Volume-4, Issue-6, November-2017
DOI: 10.21276/ijirem.2017.4.6.1

Design and Manufacturing of Micro Fabricated Planar Coils with High Turn Density

K. Anil
Mechanical Engineering, JNTUH/
Aurora Engg College,
Hyderabad, India,
ravividyuth@gmail.com

R.Dhasaratha Naik
Mechanical Engineering, JNTUH/
Aurora Engg College,
Hyderabad, India,
dasharath.jun1993@gmail.com

G. Ranjan Kumar
Mechanical Engineering, JNTUH/
Aurora Engg College,
Hyderabad, India,
Ranjan221@gmail.com

ABSTRACT
This work key point is to achieve the high turn's density without reducing the conductor section in order to limit Joule heating and ohmic losses. This paper aims to present and validate a fabrication process for the fulfilling of the aforementioned tasks addresses the design and the fabrication of small scale square planar coils with high density of turns and self inductances up to Then, an effective process flow based on polyimide (PI) and copper processing is presented, and the key aspects of the processing are discussed. Finally, the fabricated coils are characterized both electrically and morphologically, and the results are compared to the model showing good agreement with the theoretical calculations.

Keywords
Ohmic losses, heating , design, fabricated

1. INTRODUCTION
In recent years, small scale inductors have become ubiquitous in multiple fields of technology, including wireless energy transfer, inductive sensing, biomedical applications, MEMS electrical machines as well as integrated circuits (IC) in general. However, for both scaling and technological reasons, the electromagnetic properties of micro fabricated inductors are limited with respect to their macro counterparts, with lower quality factors [1] and typical inductances of the order of several *nH* for millimetres scale components. So far, a significant technological effort was dedicated to the enhancement of the performances of such devices, and lots of strategies, involving a great variety of materials and geometries, were adopted to accomplish this challenging task. While several fabrication flows aiming to obtain 3D-like structures have been proposed in recent years [2][3], planar 2D coils are still a valid option for multiple applications. For this class of devices, the improvement of the electromagnetic performances is frequently pursued by fabricating multilayer coils [4][5]. Furthermore, several authors recently developed manufacturing processes comprising the implementation of ferromagnetic materials [6][7]. In this context, a complementary strategy for the enhancement of the electromagnetic properties is to increase the turns density the coils. As a matter of fact, a high turns density might be extremely useful at different levels depending on the application. As an example, in MEMS electrical machines the possibility to increase the number of turns while still preserving the compactness of the device, is particularly attractive as a higher number of turns normally leads to a better electromagnetic coupling between the static and the movable parts [8][9]. In the same way, planar inductors designed to have high quality factors do not usually provide a high number of turns. Nevertheless, for a given section of the conductor, reducing the spacing between the turns allows to have inner spires with larger surfaces, thus increasing the contribution to the overall inductance of the device. In this context, a technological key point is to achieve the high turns density without reducing the conductor section in order to limit Joule heating and ohmic losses. This paper aims to present and validate a fabrication process for the fulfilling of the aforementioned tasks. The process is based on copper electroplating into a Polyimide (PI) mould, and it was successfully used for the manufacturing of two types of single layer square coils.

2. DESIGN

2.1. Optimization Strategy
The design strategy of a planar inductor may vary a lot, depending on the application and the contingent constraints. As for example, typical objective functions may be the quality factor, the coil shape or the magnetic coupling. Here, it was chosen to maximize the self inductance, as this particular criteria normally leads to an high density of turns, and it is therefore suitable for the demonstration of a process flow that aims to fulfil such task. Two types of square coils were considered. In order to restrain the technological domain and simplify the design, the coils dimensions were considered as fixed parameters, the number of turns being the only optimization variable. In particular, the turn width was set equal to 2 μm (type "A" coil) and 3 μm (type "B" coil). For both configurations the nominal spacing between turns was set equal to 2 μm, while the outer side of the coil was set equal to 3 *mm*. Such parameters were chosen taking into account the limits of the implied technology.

2.2. Definition of the Objective Function
Several analytic models were proposed for the calculation of self inductance of planar inductors, comprising different shapes and number of layers [10][11]. In this paper, the self inductance was determined by making use of the modified Wheelers formula [12][1].

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \quad (1)$$

In (1) the coefficients K_1 and K_2 are empirical coefficients depending on the coil shape, n is the number of turns, d_{avg} is the average diameter and ρ is the filling ratio of the coil (Figure 1).

One should notice that the formula doesn't take into account any effects activated at high frequency (*e.g.* skin and proximity effects) that are known for having an impact on self inductance The range of validity is therefore limited to low frequencies.

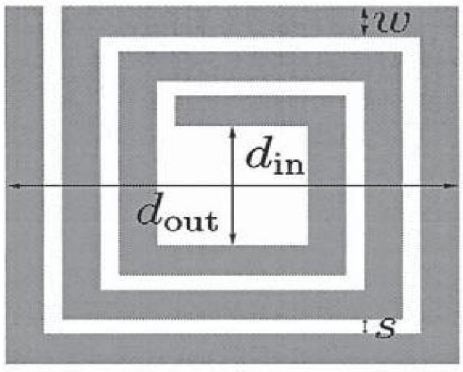

Figure 1: Parameters for the computation of the Wheeler's formula [1].

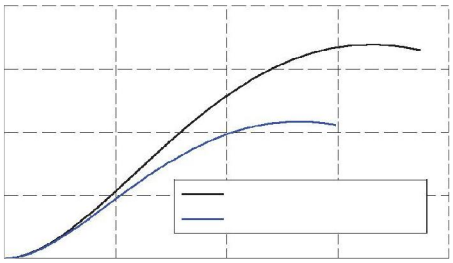

Figure 2: Self inductance as a function of turns number for type A and type B coils

Figure 2 shows the self inductance as a function of the number of turns for the two coil types according to (1). In particular, the self inductance was calculated keeping the size of the outer turn as a fixed parameter and adding the turns from the outside to the inside of the coil. As can be observed, at the beginning the self inductance tends to increase almost linearly as the number of turns increases. However, since the area of each additional loop decreases, the contribution to the overall self inductance becomes less and less significant. At the same time, the negative contribution given by the mutual inductance becomes more important [1], eventually resulting in a reduction of the coil inductance. The optimal value for the number of turns reflects this transition, and it can be obtained with ease. The characteristics of the optimized coils are reported in Table I. As will be discussed, due to the peculiarities of the fabrication process, the actual dimensions are expected to vary with respect to the nominal values.

Table 1: Optimization result

	Outer side (mm)	Spacing (μm)	Optimal number of turns	Lmax (μH)
type A	3	2	329	169
type B	3	2	263	108

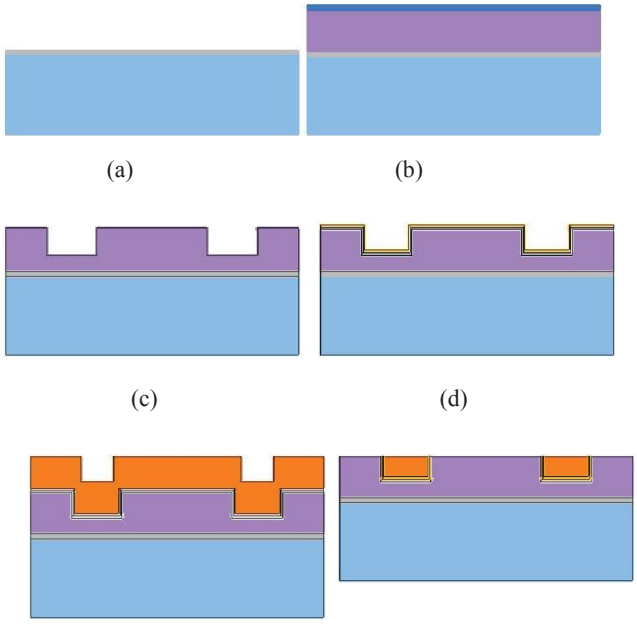

Figure 3: Schematic cross section of the process flow

3. FBRICATION

3.1 Process flow outlook

Figure 3 shows a schematic cross section of the process flow, which can be considered to be a variation of the Figure 3. Schematic of the process flow: (a) Sputtering of 150 nm Al, (b) 10 μm PI deposition + sputtering of 200 nm SiO_2, (c) PI mold structuration, (d).
Seed layer deposition, (e) electroplating, (f) CMP + IBE cleaning.
Damascene process, first established by IBM in the late 90s. It's an additive technique, consisting in etching trenches into a dielectric layer, filling the trenches with copper and then removing the copper from the entrenched area through a step of chemical mechanical polishing (CMP). While the basic principle stayed the same, multiple combinations in terms of materials (silicon, dioxides, polymers) and deposition techniques (electroplating, electro less deposition) were studied throughout the years. Here PI was chosen as the mold material due to its low-κ properties and its low internal stress, the latter being especially important due to the targeted high density of copper lines. A novel approach based on Ion Beam Etching (IBE) for the cleaning of the coil surface after the CMP step is also proposed. The fabrication steps are discussed in detail below making reference to Figure 3.

3.2 Steps (a)-(b)

The first step consists in the deposition of a 150 *nm* aluminium layer on a blank silicon wafer (Figure 3(a)). Such layer has the only function of enhancing the adhesion between the PI and the

underlying silicon. PI is then spun on the wafer surface and cured at 300 $^{\circ}C$ in a N_2 environment. Targeted thickness is equal to 10 μm. After, a 200 nm layer of SiO_2 is sputtered on the PI (Figure 3(b)) with the purpose of serving as a hard mask for PI etching. The use of a hard mask is due
to the fact that the oxygen based plasma used for PI etching is very selective (> 20 : 1) with respect to SiO_2. This allows to use sub-micrometer thick resist during the lithography process, with consequent benefits in terms of achievable resolution.

3.3. Step (c)

After lithography on a 550 nm thick photo resist, the SiO_2 hard mask is structured by mean of a CF_4 plasma. Subsequently, an oxygen plasma recipe is used for the PI etching. Such technique is highly anisotropic and allows to etch relatively deep trenches with almost vertical walls without compromising the isolation in between, which is a key point in order to obtain a high turn density. The etch depth however requires significant effort to be optimized. In fact, a deeper etch depth will result in a larger section of the conductor, leading to better electric performances in terms of ohmic losses and Joule heating. On the other hand, the etching technique is far from being 100% anisotropic and the PI walls between the trenches are also affected by the process. While a thinning of such structures with respect to their nominal value is desired, as it leads to a larger conductor section, an excessive etch depth might deteriorate them completely (Figure 4). For the given nominal insulation of 2 μm it was found an optimal etch depth around 5 μm. Once the PI etch is complete, another CF_4 plasma is used for the removal of the SiO_2 hard mask. Such step is particularly important, since any residual SiO_2 will end up in being removed during the CMP, resulting in spare particles that are most likely to cause scratches on the softer copper surface.

3.4. Step (d)-(e)

Once the PI mould is complete, the process flow provides to fill the trenches with copper. For this purpose, the electroplating technique was chosen, as it combines good trench filling properties with the possibility to deposit thick layers with relative ease. However, such technique can only be applied to conductive substrates, and since PI is a dielectric material, the preliminary deposition of a conductive seed layer (Figure 3(d)) is necessary in order to

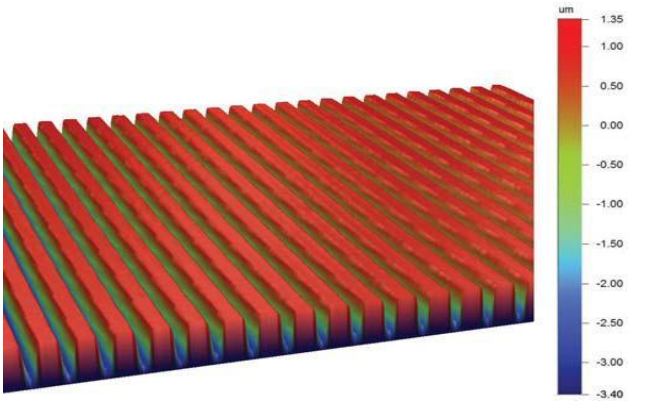

Figure 4: Optical profiler measurement performed on a B type coil after the seed layer deposition

performed right after the seed layer deposition on a type B coil. Measured etch depth is equal to 4.75 μm. The trench filling via electroplating is normally performed immediately after the seed layer deposition in order to prevent the oxidation of the surface, which might result in a poor quality of the electroplated copper as well as adhesion issues.

3.5 Step (f)

After the electroplating, the copper in excess is removed with a CMP step (Figure 3(f)). During the process a wide variety of defects may be induced on the wafer, including contamination issues, scratches [11], slurry residues as well as design dependent defects like dishing and erosion. Among the others, the absorption of the sub-micron slurry particles on the copper surface (6) was found to be a major issue, as the non conductive nature of such particles compromise the contact resistance of the coils. Post-CMP cleaning is normally based on brush scrubbing [12], and a number of efforts were made in order to increase the efficiency of the process, focusing both on the modelling and the chemicals involved . Here, a completely different approach based on IBE was chosen. The technique is based on the generation of a broad band of Argon ions from an ICP source. The ions are then accelerated and directed towards the substrate, where the materials are etched by purely mechanical sputtering. With respect to the brush scrubbing, the IBE cleaning offers several advantages. First of all, assumed that the ion beam etcher is provided, the process doesn't require a dedicated setup. Also, since no chemicals are involved, the etching being purely physical, the optimization of the procedure is relatively simple. At the same time any issues related to the compatibility of the materials are drastically reduced. Finally, a dry technique is particularly useful when working with copper, since it tends to get oxidized easily in moist environments. However, a major drawback is that the ion beam has no selectivity with respect to the the silica particles, so that the PI/copper structures are also affected by the process. An attentive control of the cleaning parameters.

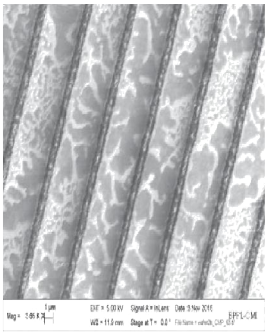

Figure 5: Surface contamination by slurry silica particles after CMP

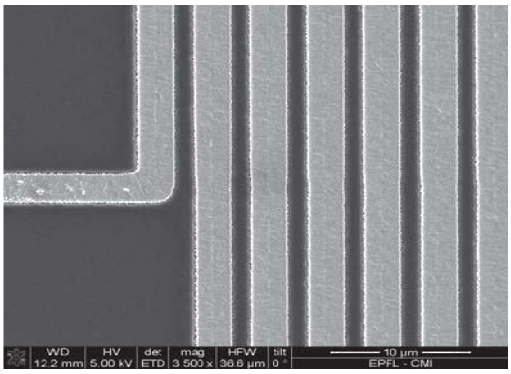

Figure 6: Aerial view of a finished coil

Beam energy and the duration of the process is thus needed in order to preserve the coil functionality. For the same reason the method is not suitable whenever the application requires a high smoothness of the surface, since the etched silica particles tend to leave footprints on the underlying copper. Figure 6 shows a detail of a completed coil after the IBE cleaning, while an aerial view of a finished coil can be observed in Figure 6.

4. TCHARACTERIZA AND MEASUREMENT

4.1. Morphology

The coils were characterized by using a Focused Ion Beam (FIB) in order to obtain and analyze the cross section of the conductor. As can be observed, the PI mould is perfectly filled with copper. Since the etching rate is higher for larger structures, the type A coil, which was designed with a smaller turn width, shows a lower etch depth (around 4 µm) than the type B coil (around 4.5 µm). In the same way, the reduction of the isolation width due to the lateral etching is also less pronounced. The final aspect ratio of the isolation is equal to 1 : 3 for type A and 1 : 4.5 for type B coils. Since the spacing between turns is reduced, the conductor section is increased accordingly. The thickness of the conductor is slightly lower with respect to the measured etch depth of the PI mould. This is a direct effect of the the dishing occurred during CMP as well as the IBE on copper during cleaning process. The discrepancy is however <220 nm and it can be considered negligible with respect to the total thickness of the conductor. The resulting turn density is equal to 0.25 lines/µm and 0.20 lines/µm for type A and type B coils respectively.

4.2 Electrical Behaviour

Several models were proposed for the characterization of the electrical behaviour of planar coils [12]. Here, the measurements on the coils were performed with an Agilent 4294A precision impedance analyzer, taking the lumped parameter circuit in Figure 10 as a reference. The frequency was swept in a range comprised between few kHz and 800 kHz. Such range was chosen in order to reduce the incertitude on the measure while still not activating any high frequency effects which are not taken into account in the theoretical model. Due to the low frequency applicability of the model, the influence of the parasitic capacitance C_p, will not be discussed.

The theoretical DC resistance of the devices can be cal culated starting from the section of the conductor measured through FIB analysis. Since at low frequency such value can be considered to be proportional to the resistivity of the material, a comparison with the measured values (Table II) allows to estimate the resistivity of the conductor. Best fit is obtained for a resistivity around $2.0 \cdot 10^{-8}\ \Omega \cdot$ m. As for the self inductance, the results are listed in Table III. As can be observed, the measurements are in good agreement with the theoretical calculations, showing a discrepancy below 7%.

5. CONCLUSION

Two types of planner coils with high turn density were design and fabricated. First the optimal number of turns was found making use of the modified Wheeler's formula.

REFERENCES

[1] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," IEEE Journal of Solid-State Circuits, vol. 34, no. 10, pp. 1419–1424, Oct 1999.

[2] L. Gu and X. Li, "High-q solenoid inductors with a cmos-compatible concave-suspending mems process," Journal of Microelectromechanical Systems, vol. 16, no. 5, pp. 1162–1172, Oct 2007.

[3] V. Badilita, K. Kratt, T. Burger, J. G. Korvink, and U. Wallrabe, "3d high aspect ratio, mems integrated micro-solenoids and helmholtz micro-coils," in TRANSDUCERS 2009 - 2009 International Solid-State Sensors, Actuators and Microsystems Conference, June 2009, pp. 1106– 1109.

[4] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," IEEE Journal of Solid-State Circuits, vol. 34, no. 10, pp. 1419–1424, Oct 1999.

[5] L. Gu and X. Li, "High-q solenoid inductors with a cmos-compatible concave-suspending mems process," Journal of Microelectromechanical Systems, vol. 16, no. 5, pp. 1162–1172, Oct 2007.

[6] V. Badilita, K. Kratt, T. Burger, J. G. Korvink, and U. Wallrabe, "3d high aspect ratio, mems integrated micro-solenoids and helmholtz micro-coils," in TRANSDUCERS 2009 - 2009 International Solid-State Sensors, Actuators and Microsystems Conference, June 2009, pp. 1106– 1109.

[7] Tavel, P. 2007. Modeling and Simulation Den. AK Peters Ltd., Natick, MA.

[8] Sannella, M. J. 1994. Constraint Satisfaction and Debugging for Interactive User Interfaces. Doctoral Thesis. UMI Order Number: UMI Order No. GAX95-09398., University of Washington.

[9] Forman, G. 2003. An extensive empirical study of feature selection metrics for text classification. J. Mach. Learn. Res. 3 (Mar. 2003), 1289-1305.

[10] Brown, L. D., Hua, H., and Gao, C. 2003. A widget framework for augmented interaction in SCAPE. In Proceedings of the 16th Annual IJIREM Symposium on User Interface Software and Technology (Vancouver, Canada, November 02 - 05, 2003). UIST '03. IJIREM, New York, NY, 1-10. DOI= http://doi.IJIREM.org/10.1145/964696.964697.

[11] Yu, Y. T. and Lau, M. F. 2006. A comparison of MC/DC, MUMCUT and several other coverage criteria for logical decisions. J. Syst. Softw. 79, 5 (May. 2006), 577-590. DOI= http://dx.doi.org/10.1016/j.jss.2005.05.030.

[12] Spector, A. Z. 1989. Achieving application requirements. In Distributed Systems, S. Mullender, Ed. IJIREM Press Frontier Series. IJIREM, New York, NY, 19-33. DOI= http://doi.IJIREM.org/10.1145/90417.90738.

